A19 26. (AMENDED) The computer-usable medium of Claim 25 wherein said microcontroller is designed according to a programmable single-chip architecture.

A20 34. (AMENDED) The GUI of Claim 31 wherein said tasks comprise tasks for designing a microcontroller according to a programmable single-chip architecture.

IN THE DRAWINGS

Applicant respectfully requests approval of the drawing change to Fig. 2A shown in the attached Request for Approval of Drawing Changes.

AMENDMENTS WITH CHANGES SHOWN:

IN THE SPECIFICATION

Please replace the paragraph beginning at page 2, line 7 with the following new paragraph:

To overcome these problems, microcontroller suppliers (specifically, Cypress MicroSystems in Bothell, Washington) have started to offer standard parts that combine a microprocessor with several user-configurable "building blocks." These building blocks may be assembled, configured and programmed to form many standard microprocessor peripherals, as well as to form unique peripherals as may be required by a specific application. Thus, a user can tailor a microcontroller to meet his or her specific requirements, in less time and at less cost than through other means. A microcontroller assembled from these building blocks is referred to herein as a programmable <u>single-chip</u> system [on a chip (PSoC)]. Additional information regarding [PSoCs] <u>such a microcontroller</u> is provided in the co-pending, commonly-owned US Patent Application, Attorney Docket No. CYPR-CD00232, Serial No. [________] <u>10/033,027</u>, filed October 22, 2001, by W. Snyder, and

entitled "Programmable Microcontroller [Programmable System on a Chip] Architecture," hereby incorporated by reference.

Please replace the paragraph beginning at page 4, line 17 with the following new paragraph:

Thus, what is needed is a method or system that can help guide a user through a series of tasks in an orderly manner while facilitating movement between tasks. What is also needed is a method or system that can satisfy the above need and that can be used for the design of microcontrollers, such as microcontrollers of the [PSoC] design mentioned above. The present invention provides a novel solution to these needs.

Please replace the paragraph beginning at page 8, line 9 with the following new paragraph:

Figure 2A is a block diagram of an exemplary programmable single-chip system [on a chip (SoC)] architecture used with one embodiment of the present invention.

Please replace the paragraph beginning at page 8, line 12 with the following new paragraph:

Figure 2B is a block diagram of an exemplary arrangement of [SoC] programmable system blocks used with one embodiment of the present invention.

Please replace the paragraph beginning at page 13, line 11 with the following new paragraph:

The present invention is described in the context of a software tool, portions of which are comprised of computer-readable and computer-executable instructions which reside, for example, in computer-usable media of a computer system such as that exemplified by Figure 1. The present invention is primarily described as being used with a tool for designing, configuring, programming, compiling, building (assembling), emulating, and debugging an embedded microcontroller, in particular a class of microcontrollers that provide analog and/or digital subsystems comprising many

dynamically configurable blocks. An example of this class is referred to herein as a programmable microcontroller architecture [system on a chip (PSoC)]. Additional information regarding [PSoCs] such an architecture is provided in the co-pending, commonly-owned US Patent Application, Attorney Docket No. CYPR-CD00232, Serial No. [______] 10/033,027, filed October 22, 2001, by W. Snyder, and entitled "Programmable Microcontroller [Programmable System on a Chip] Architecture," hereby incorporated by reference.

Please replace the paragraph beginning at page 14, line 4 with the following new paragraph:

Figure 2A is a block diagram of an integrated circuit (or microcontroller) 210 that exemplifies a microcontroller which uses [the PSoC] a programmable architecture. In the illustrated embodiment, integrated circuit 210 includes a system bus 211, and coupled to bus 211 are synchronous random access memory (SRAM) 212 for storing volatile or temporary data during firmware execution, central processing unit (CPU) 214 for processing information and instructions, flash read-only memory (ROM) 216 for holding instructions (e.g., firmware), input/output (I/O) pins 218 providing an interface with external devices and the like, and system [on a chip (SoC)] blocks 225. The [SoC] system blocks 225 include analog blocks and digital blocks.

Please replace the paragraph beginning at page 14, line 15 with the following new paragraph:

Referring to Figure 2B, an embodiment of [SoC] system block 225 is depicted in greater detail. In this embodiment, [SoC] system block 225 includes an analog functional block 230, a digital functional block 240, and a programmable interconnect 250. Analog block 230 includes, in the present embodiment, a matrix of interconnected analog blocks A1 through AN. The number N may be any number of analog blocks. Likewise, digital block 240 includes, in the present embodiment, a matrix of interconnected digital blocks D1 through DM. The number M may be any number of digital blocks. The analog blocks A1 through AN and the digital blocks D1 through DM

are fundamental building blocks that may be combined in different ways to accomplish different functions. Importantly, different combinations of blocks, producing different functions, may exist at different times within the same system. For example, a set of blocks configured to perform the function of analog-to-digital conversion may sample a signal. After processing that signal in the digital domain, those same blocks (perhaps in conjunction with a few others) may be recombined in a different configuration to perform the function of digital-to-analog conversion to produce an output signal.

Please replace the paragraph beginning at page 16, line 4 with the following new paragraph:

With reference next to Figure 3, process 300 illustrates exemplary steps used by a microcontroller design tool in accordance with one embodiment of the present invention. The purpose of process 300 is to configure, program, compile, build, emulate and debug a customized microcontroller (a "target device") based on the integrated circuit 210 and [SoC] <u>system</u> blocks 225 of Figures 2A and 2B.

Please replace the paragraph beginning at page 17, line 7 with the following new paragraph:

In step 310, applicable "user modules" are selected. A user module, as used herein, is a preconfigured function that may be based on more than one [SoC blocks] <u>system block</u>. A user module, once placed and programmed, will work as a peripheral on the target device. At any time in process 300, user modules may be added to or removed from the target device.

Please replace the paragraph beginning at page 17, line 13 with the following new paragraph:

The selected user modules can then <u>be</u> "placed" or "mapped" onto the [SoC] <u>system</u> blocks 225 of Figure 2B. Once a user module is placed, its parameters can be viewed and modified as

needed. Global parameters used by all of the user modules (for example, CPU clock speed) can also be set.

Please replace the paragraph beginning at page 17, line 18 with the following new paragraph:

Continuing with step 310 of Figure 3, interconnections between the selected user modules can be specified, either as each user module is placed or afterwards. The pin-out for each [PSoC] programmable system block can be specified, making a connection between the software configuration and the hardware of the target device.

Please replace the paragraph beginning at page 21, line 4 with the following new paragraph:

In the present embodiment, some of the elements are always active, regardless of which task is being performed (or which window or workspace is open). As depicted in Figure 4A, the three elements A, B and C are active at all times, and the other elements are not active. For example, the microcontroller design tool described in conjunction with Figure 3 is, in one embodiment, divided into at least three subsystems: a Device Editor subsystem, an Application Editor subsystem, and a Debugger subsystem. In essence, the Device Editor subsystem implements steps 310-320 of Figure 3, the Application Editor subsystem implements steps 330-340 of Figure 3, and the Debugger subsystem implements step 360 of Figure 3. According to the present invention, an element is associated with each of these subsystems, and the element for each subsystem is always active, regardless of which subsystem is being used for the task at hand. Thus, a user can readily move between various tasks (or windows or workspaces) by selecting the appropriate active element. For example, in the microcontroller design tool, the user can move from the Debugger subsystem back to the Device Editor subsystem without having to pass through the Application Editor subsystem.

Please replace the paragraph beginning at page 21, line 21 with the following new paragraph:

Another feature of the [presentation] present invention is that the graphic elements are rendered in GUI 400 in locations that correspond to the logical order in which tasks should be performed. For example, as described above, in the microcontroller design tool, the Device Editor subsystem implements steps 310-320 of Figure 3, the Application Editor subsystem implements steps 330-340 of Figure 3, and the Debugger subsystem implements step 360 of Figure 3. In accordance with the present invention, element A is associated with the Device Editor subsystem, element B with the Application Editor subsystem, and element C with the Debugger subsystem. The order of the graphic elements is used to suggest to the user the order in which the subsystems are to be accessed.

Please replace the paragraph beginning at page 22, line 16 with the following new paragraph:

Figure 4B is described further by way of example. In the microcontroller design tool, a user can select a user module and place it using the Device Editor subsystem (refer to step 310 of Figure 3). To accomplish this, the user selects element A (for example) to implement the Device Editor subsystem. In response to this selection, elements for the user module selection task and for the user module placement task (e.g., elements Al and A2) are activated. Other elements may also be activated for the other tasks that can be performed using the Device Editor subsystem.

Please replace the paragraph beginning at page 23, line 1 with the following new paragraph:

Thus, similar to that described above, elements are presented to the user in such a way so as to guide the user through the tasks in a logical order; for example, the user module selection task and the user module placement task are not activated until the user implements the Device Editor subsystem. As well, the elements are placed to suggest to the user a logical order for performing the tasks. That is, for example, the elements for the user module selection task and for the user module placement task are proximate to each other, implying a relationship between the tasks. Also, the

element for the user module selection task is placed to the left of the element for the user module placement task, implying an order in which the tasks should be performed.

Please replace the paragraph beginning at page 25, line 7 with the following new paragraph:

It is appreciated that, in response to user selection of element B, not all of the elements A1-A4 may be deactivated. For example, element A1 may remain active. In this manner, a shortcut is created between tasks. For instance, in the microcontroller design tool in which element A is associated with the Device Editor <u>subsystem</u> and element B is associated with the Application Editor <u>subsystem</u>, a user may move from a task in the Application Editor <u>subsystem</u> directly to a task in the Device Editor <u>subsystem</u> without traversing through all of the intervening tasks. For example, the user can move directly between a task associated with any of the elements B1-B4 to the task associated with element A1, and vice versa. Thus, the user does not have to leave a task in the Application Editor <u>subsystem</u>, enter the Device Editor <u>subsystem</u>, next enter a specific task within the Device Editor <u>subsystem</u>, and then reverse these steps to return to the task in the Application Editor <u>subsystem</u>; instead, the user moves directly to the task in the Device Editor <u>subsystem</u>, then directly back to the task in the Application Editor <u>subsystem</u>. However, the user is still presented with only a limited number of choices that are intelligently selected and enforced by activating and deactivating certain elements. Thus, as opposed to a conventional wizard approach, a user has greater flexibility and freedom of movement, but the user is still provided with a degree of organization and guidance, in contrast to a conventional free form approach.

<u>IN THE CLAIMS</u>

6. (AMENDED) The method of Claim 5 wherein said microcontroller is designed according to a programmable [system on] <u>single-</u>chip architecture.

16. (AMENDED) The computer system of Claim 15 wherein said microcontroller is designed according to a programmable [system on] <u>single-</u>chip architecture.

26. (AMENDED) The computer-usable medium of Claim 25 wherein said microcontroller is designed according to a programmable [system on] <u>single-</u>chip architecture.

34. (AMENDED) The GUI of Claim 31 wherein said tasks comprise tasks for designing a microcontroller according to a programmable [system on] <u>single-</u>chip architecture.

SUPPORT FOR AMENDMENTS

Support for the amendments herein can be found throughout the specification as originally filed and in co-pending, commonly-owned US Patent Application Serial No. 10/033,027, filed October 22, 2001. The present amendment intends to remove references to the trademarks of Cypress MicroSystems, Inc. (see, e.g., M.P.E.P. § 608.01(v) and the attached printouts from http://tess.uspto.gov/, notably the "PSOC" trademark registration information therein, and http://www.cypressmicro.com/corporate/CY_Announces_nov_13_2000.html.) No new matter is introduced.

REMARKS

Claims 1-30 are presented for consideration in the present application, which is now believed to be in condition for examination. Early notice to that effect is earnestly solicited.

Respectfully submitted,

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Mark Drawing Code	(1) TYPED DRAWING
Serial Number	75951037
Filing Date	March 3, 2000
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Attorney of Record	John Weber
Type of Mark	TRADEMARK
Register	PRINCIPAL
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CYPRESS MICROSYSTEMS UNVEILS PROGRAMMABLE SYSTEM-ON-A-CHIP FOR EMBEDDED INTERNET, COMMUNICATIONS AND CONSUMER SYSTEMS

PSoC™ Devices Integrate Programmable Analog and Digital Functions To Simplify Design Of Wireless, Handheld, Data Communicati ns, and Industrial Systems

WOODINVILLE, Wash., November 13, 2000 - Cypress MicroSystems, a subsidiary of Cypress Semiconductor, today introduced a family of programmable system-on-a-chip (PSoC™) devices, designed to implement a single, configurable device on MCU-based system boards. As general purpose solutions, PSoC devices are targeted for implementation in embedded applications, including audio, wireless, handheld, data communications, Internet control, industrial, and consumer systems.

PSoC devices integrate a fast microcontroller, SONOS™-based (Silicon Oxide Nitride Oxide Silicon) Flash memory and SRAM, and programmable arrays of analog and digital system functions - known as PSoC blocks - in low-cost, small-footprint packages. To save designers time, Cypress Microsystems also offers User Modules - pre-designed peripherals comprised of PSoC blocks. By selecting a PSoC with the needed resource combination of memory, PSoC blocks and pins, designers have a device that reduces costs by eliminating external chips and simplifying system design.

"Today there are thousands of different 8-bit microcontrollers on the market, and designers still have trouble finding one that is a perfect fit for their application. In addition, embedded applications require analog peripherals that usually call for additional external devices," said Mike Polen, Cypress MicroSystems's vice president of marketing. "Engineers know that the perfect solution is a custom-designed system-on-a-chip, but custom microcontrollers, ASICs and PLDs are expensive,.require very large volumes or call for specialized design skills."

"In contrast, the Cypress Microsystems PSoC solution offers custom configurations, takes no time or special expertise to create, incurs no NRE, and integrates both analog and digital functions," continued Polen. "These factors make the cost of the PSoC solution competitive with standard microcontrollers."

SONOS - a proprietary Cypress process technology - is key to Cypress Microsystems's system-on-a-chip. SONOS is a cost-effective, electrically-erasable, programmable, non-volatile memory structure that speeds time-to-market at a cost that is comparable with commodity devices. SONOS is also being implemented in Cypress Semiconductor's frequency timing generators, USB controllers and intelligent control network devices.

About PSoC blocks and User Modules

After a review of the peripherals found in microcontrollers and the analog ICs used in typical designs, Cypress Microsystems engineers selected a variety of digital and analog peripherals, then created PSoC blocks, or system-on-a-chip blocks, and integrated them into each PSoC device. Users select the functions they need and configure the PSoC blocks on the PSoC device accordingly.

Digital PSoC blocks are 8-bit peripherals that can be programmed to perform a variety of functions by changing the contents of a few registers. They can be configured as timers, controllers, serial communications ports, CRC generators, or pseudo-random number generators. They can be connected in series to handle more complex functions - for example, a 24-bit timer is three connected 8-bit PSoC blocks acting as timers.

Analog PSoC blocks consist of programmable operational amplifier circuits that can be configured to perform a set of typical analog peripheral functions. Analog PSoC blocks can be programmed by setting a few registers to internconnect and trim the appropriate operational amplifier circuit to create the desired result. Among the typical peripherals that can be created are amplifiers, DACs, ADCs, analog drivers, and high-, low- and band-pass filters.

To eliminate the need for customers to understand PSoC blocks in-depth and further shorten development time, Cypress Microsystems developed User Modules, preconfigured peripherals created from PSoC blocks. User Modules allow customers to select the functions they need and automatically integrate the necessary PSoC

blocks into their PSoC device.

Software Support

Cypress Microsystems will offer PSoC Designer™, a complete development system to support the PSoC device. The system will include a C compiler and assembler, a linking and debugging tool, an in-circuit emulator, and the Device Editor™.

Designers can use the Device Editor and its graphical interface to configure a PSoC device by dragging the desired peripherals or functions - from a library of User Modules - into the part. The selected User Modules are then automatically mapped onto the available PSoC blocks.

On-chip Flash program memory stores each PSoC device's parameters, allowing the user to reprogram the device during production, during system test or in the field. PSoC devices may even be self-reprogrammed remotely.

"PSoC devices are like a screwdriver with replaceable bits," stated Nathan John, Cypress Microsystems's director of marketing. "They can be configured and reconfigured as the design progresses and functional requirements change. They provide a core set of analog and digital functions that eliminate the need for additional devices. And they can be programmed to custom-fit any application."

Availability and Pricing

Cypress Microsystems will initially offer the following PSoC devices:

Part Number	Max. Speed	Package	Samples	Production	Price (Q 1,000)
CY8C25122	24 MHz	8-pin DIP	Q1 2001	Q1 2001	$ 1.76
CY8C26233	24 MHz	20-pin DIP 20-pin SOIC 20-pin SSOP	Q1 2001	Q1 2001	$ 2.21
CY8C26443	24 MHz	28-pin DIP 28-pin SOIC 28-pin SSOP	Q4 2000	Q1 2001	$ 2.79
CY8C26643	24 MHz	48-pin DIP 48-pin SSOP 48-pin TQFP	Q1 2001	Q1 2001	$ 3.53

About Cypress Microsystems

Cypress Microsystems designs, develops, manufactures and markets high-performance, field programmable integrated micro-based solutions for high-volume embedded control functions in computer, communications, consumer and control applications. Established as a subsidiary of Cypress Semiconductor Corporation in the fourth quarter of 1999, Cypress Microsystems's stockholders are its employees and Cypress Semiconductor. The close association with Cypress Semiconductor allows access to their process and design technology, and field sales and applications forces. Cypress Microsystems is based near Seattle in Woodinville, Washington.

The Cypress Microsystems PsoC™ family of programmable system-on-a-chip devices will replace many MCU-based system boards with one single-chip, programmable PSoC. A single PSoC device provides a fast microcontroller, SONOS™ FLASH and SRAM memory, and configurable analog and digital peripheral blocks in a range of convenient pin outs and memory sizes. This new product family will bring the cost and time-to-market advantages of programmable technologies, such as CPLDs and FPGAs, to the emerging system-on-a-chip marketplace.

More information about Cypress Microsystems and its products can be accessed through its Web site at www.cypressmicro.com.

"Safe Harbor" Statement under the Private Securities Litigation Reform Act of 1995: Statements in this press release regarding Cypress Semiconductor's business that are not historical facts are "forward-looking statements" involving risks and uncertainties, including but not limited to: the effect of global economic conditions, shifts in supply and demand, market acceptance, the impact of competitive products and pricing, product development, commercialization and technological difficulties, and capacity and supply constraints. Please refer to Cypress Semiconductor's Securities and Exchange Commission filings for a discussion of such risks.

PSoC, PSoC Designer, and Device Editor are trademarks of Cypress Microsystems SONOS is a trademark of Cypress Semiconductor.